CSCE 4610: Computer Systems Architecture

You May Want To Know

Instructor: Krishna Kavi
My Office: F 278 Discovery Park
My Phone: 940-369-7216
My Email: krishna.kavi@unt.edu
My Web: http://csrl.cse.unt.edu/~kavi/
My Office Hours;
Tuesdays 9:00-10:30am
Thursdays 1:00-2:30pm
(Other times by appointment only)

TA: TBD

Tentative Breakdown Of Course Grades
(I reserve the right to make changes to this breakdown)

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<td>2 Mid Semester Exams</td>
<td>40%</td>
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<td>Final</td>
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<td>Homework Assignments</td>
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<td>Term Project</td>
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<td>Discretion</td>
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The purpose of this course is to provide you with a solid foundation in computer systems architecture. This course is generally considered as a foundation to further study and research in computer systems. We will survey several different approaches to designing a single CPU that can aid in building a parallel processor. We will investigate instruction level parallelism, branch prediction techniques, various cache organization, multithreaded architectures, cache coherency and their impact on parallel processing.

Prerequisites: CSCE 2610, CSCE 3612 or CSCE 3600

Primarily, I would like to see that you know how a basic CPU works, assembly language programing in MIPS (or ARM) instruction, memory organization, ALU (including multiplication, division and floating point algorithms), and some understanding of compilers and runtime support. Operating system concepts like process scheduling, virtual memory, protection domains, etc.

Exams and Grading Policies: All my exams (mid-semester and final) are "open-book" format. The final exam is not comprehensive. I grade every exam using a "relative point" system. For each problem, I select the best among all the solutions presented by the students (which gets the highest grade) and grade all the others relative to the best solution.
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Course Outline
(I reserve the right to change the order of some topics based on need)

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1. Introduction and Background
   What is computer architecture
   Instruction sets, control unit
   Performance evaluation

2. Memory Systems
   Memory hierarchy
   Cache memory designs
   Improving cache performance
   Main memory and Virtual memory
   DRAM and SSD technologies

3. Pipeline and out of order execution
   Basic design of pipelines
   Data and control hazards
   Branch prediction and dynamic scheduling
   Superscalar and multiple issue processors
   VLIW or EPIC

4. Shared Memory Multiprocessors
   Mutual Exclusion and Synchronization
   Cache Coherency Problem and Solutions
   Distributed Shared Memory Systems

5. Dataflow and multithreaded architectures
   Dataflow model of computation
   What is multithreading Scheduled Dataflow
   SMT and Hyper Threading

6. Low Power Issues


Other Useful Books: