Reconfigurable Logic  
CSCE 3730, Section 001  
Fall 2018

Class Timings: Monday and Wednesday 5:30 PM – 6:50 PM, NTDP B155

Instructor: Robin Pottathuparambil (Email: rpottath@unt.edu, Office: NTDP F263, Office hours: Tuesday and Thursday 4:00 PM – 6:00 PM or by appointment)

Instructional Assistant: Charles Goff, Email: charlesgoff2@my.unt.edu, Help Hours: F243 (Monday 10:30 AM to 1:30 PM and Wednesday 10:30 AM to 12:30 PM)

Course Webpage: All the course related material will be posted on the course webpage which is available through Canvas (https://unt.instructure.com).

Course Outcomes:
- Understand the concept of reconfigurable logic.
- Know how FPGA (most popular reconfigurable device) is designed.
- Have an overall view of Computer Aided Design (CAD) for FPGA.
- Understand specific algorithms utilized in technology - mapping, placement and routing.
- Learn how to use the hardware description language - VHDL to simulate and synthesis digital circuit system.
- Capable of using commercial CAD tools to design and simulate digital circuits.

Program Outcome Mapping:
- An ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics
- An ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions
- An ability to acquire and apply new knowledge as needed, using appropriate learning strategies.


Catalog Description: Prerequisite: CSCE 2610. Advanced concepts in Boolean algebra, use of hardware description languages as a practical means to implement hybrid sequential and combinational designs, digital logic simulation, rapid prototyping techniques, and design for testability concepts. Focuses on the actual design and implementation of sizeable digital design problems using representative Computer Aided Design (CAD) tools.

Topics:
- Fundamentals of digital logic & IC design
- FPGA overview
- Combinational logic design - fundamentals and modeling using VHDL
- Sequential logic design - fundamentals and modeling using VHDL
- Platform FPGA
Grading:

<table>
<thead>
<tr>
<th></th>
<th>Percentage</th>
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<tbody>
<tr>
<td>Homework</td>
<td>12%</td>
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<tr>
<td>Quizzes</td>
<td>12%</td>
</tr>
<tr>
<td>In-Class Activity</td>
<td>5%</td>
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<tr>
<td>Lab assignments</td>
<td>20%</td>
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<tr>
<td>ePortfolio Submission</td>
<td>1%</td>
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<tr>
<td>Midterm Exam (10/15/2018)</td>
<td>20%</td>
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<tr>
<td>Comprehensive Final Exam (12/10/2018)</td>
<td>30%</td>
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**Homework:** Homework will be in the form of problem sets with a due date one week after it is assigned. Homework will be assigned on Mondays as per the schedule. **No late homework will be accepted.** Homework must be done individually (you will learn the most from this). Any evidence of group participation or direct copying from unauthorized sources (Example: previous year’s solutions, textbook solutions, Wikipedia, and websites) will be interpreted as academic dishonesty. There will be six to seven homework assignments.

**Quizzes:** There will be six to seven pop quizzes given throughout the semester. The pop quizzes can be given any time during the class. These will be to reward students who consistently show up to class but will be more than just attendance points.

**Recitations:** The recitation section are on Monday starting from 10:30 AM to 1:30 PM and it is not mandatory. The TA and the peer mentor will be available at that time in F243 to help you with the labs.

**Experiential Learning:** It’s a process of learning where the you will be learning through experience and is designed such a way that you learn through reflection. This is also called as experiential education. To implement this, we will be using Kolb’s experiential learning model where you will be given an in-class activity or a hands-on lab and you will be asked to reflect on the experience and then this experience is used to do similar activities. The two experiential learning assignments that we will be involved are: In-class activity and hands-on labs.

- **In-class Activity:** There will be five to six in-class activity that will reinforce the concepts that we learned in the class. These in-class activities will be scheduled during the class timing. During each in-class activity you will form a team (two or three team members) and try to answer questions related to a specific topic. Once you answer the questions, the solutions will be discussed in the class and you will be provided with a chance to correct the solutions. Once you correct the solutions you will be then asked to answer some questions related to the reflection of your learning.

- **Lab Assignments:** Lab assignments are an integral part of the course and are intended to provide hands-on experience in the application of the design techniques discussed in lecture. Lab assignments will be assigned on Wednesdays as per the schedule and with a due date of two weeks after it is assigned. There will be five to six lab assignments assigned. Each of the lab assignment will be used to build the next lab. The last lab will be a final project with most of the pieces completed in the previous labs. Lab assignments must be done individually and can be done in NTDP F243/F270. Any evidence of group participation will be interpreted as academic dishonesty.

- **ePortfolio:** All students are required to create a foliotek profile page through Canvas. You will be uploading a two-page documentation regarding your final project. You will be provided with a template of the documentation that is needed. This documentation will be then graded for the
aspect of critical thinking. The evaluation will be made available to you so that you can improve
your critical thinking skills. A rubric for grading will also be given to you. You need to complete
the ePortfolio assignment to receive credit for it.

Exams: There will be a midterm exam and a final exam. Mobile phones are not permitted. Exams will
include material from the lecture, the readings, homework, and lab assignments. Final exam will be
comprehensive. Exam dates are:

- Midterm Exam: Monday, October 15th, 2018 5:30 PM – 6:45 PM, NTDP B155
- Final Exam: Monday, December 10th, 2018 5:30 PM – 7:30 PM, NTDP B155

Missing Classes/Assignments/Exams: Attendance at all exams is mandatory. Throughout the semester, a
student may miss classes, assignments, quizzes, or exams due to many reasons. Most of the reasons will
not be accepted as an "excused" absence. Assignments, quizzes, or exams can be made-up only under
extraordinary circumstances and only when notification is given to me before the quiz or exam is
administered. A no-show for a quiz or exam without prior notification and a verifiable excuse
(appropriate official documentation) results in a grade of zero for that quiz or exam.

Disputing Grades: If you have a dispute with how an assignment, quiz, or exam is graded, you should
get the solution to the lab assignment, quiz, or exam off the class web site and examine it. If you really
believe that your answer is correct (matches the answer given in the solution), contact the grader and
discuss it with him. The grader will listen to your concern, and act on it, at their discretion. In any case,
they will sign the assignment verifying that they saw it again. The lab assignments will not have solutions
posted, so contact the grader for disputing the grade if you have met all the requirements of the lab
assignment and you have lost points. Note that instructor or grader addition errors should follow the
above procedure. Assignment, quiz, exam, and homework grades are disputable for one week from the
day the grades were assigned on Canvas.

Class Policies: Please note that portable phones, pagers, and late arrivals are disruptive to the instructor
and to your peers. The use of cell phones, beepers, or communication devices is disruptive and is
therefore absolutely prohibited during class. Turn off your cell phone while in class. If I catch you using
these devices, your final grade will be reduced by 10 points for each and every transgression and you will
be asked to leave the class. Except in emergencies, students using such devices must leave the classroom
for the remainder of the class period. I know that some of you may wish to take notes directly on your
computer and I have no problem with that. If, however, you choose to access your email, search the web,
play solitaire or other games, or instant messenger your friends during class, you will have 10 points
deducted from your final grade for each and every transgression. This penalty will be at the sole
discretion of the instructor. If I am late arriving to class, it will be because of circumstances beyond my
control. You are expected to remain for 20 minutes past the scheduled class start time while I attempt to
communicate my situation and relay instructions.

Syllabus Revisions: This syllabus may be modified as the course progresses. Notice of such changes will
be by email or announcement in class.

Course Policies: You are expected to spend at least 10 hours per week for this course. Keep all your
graded assignments, quizzes, and tests for study and review. You should track your own progress on
Canvas and be aware of current grades throughout the term. I will make all the effort to return the graded
assignments, but it’s your responsibility to collect back the graded assignments from the grader or the
instructor if it is not given back to you. Final grading will be done as follows. A: >= 90%, B: >= 80% and
< 90%, C: >= 70% and < 80%, D: >= 60% and < 70% and F: < 60%. Grades will be curved if necessary.
Grades cannot be changed after they have been electronically entered into the university’s system except
for instructor error. Any extenuating circumstances that may adversely affect your grade must be brought to my attention before the final course grades are recorded. To be considered, such circumstances must be unusual, unavoidable, and verifiable.

Disability Services/Special Needs: UNT complies with all federal and state laws and regulations regarding discrimination including the Americans with Disability Act of 1990 (ADA). If you have a disability and need a reasonable accommodation for equal access to education or services, please contact the Office of Disability Accommodation. Please initiate this process and inform me during the first two weeks of class.

Academic Dishonesty: All the provisions of the University code of academic integrity apply to this course. In addition, it is my understanding and expectation that your signature on any test or assignment means that you neither gave nor received unauthorized aid. For homework and lab assignments, while discussion is allowed, direct copying is not, and students must turn in individual submissions. All students are required to know, observe and help enforce the UNT Code of Student Academic Integrity. Cheating will result in disciplinary action according to UNT Policy 18.1.16. The penalty for a first offense can range from a formal warning to an ‘F’ for the course. Regardless of the penalty imposed, a record of the offense will be kept in the Office of the Dean of Students.

Student Perceptions of Teaching (SPOT): Student feedback is important and an essential part of participation in this course. The student evaluation of instruction is a requirement for all organized classes at UNT. The short SPOT survey will be made available November 19 – December 6 to provide you with an opportunity to evaluate how this course is taught.

ABET Survey: Towards the end of the course, the students will be asked to ABET exit survey which will help instructors to quantitively measure whether the students met the course outcomes stated in the course syllabus. This survey will be administered during the last week of classes.

Tentative Course Schedule:

<table>
<thead>
<tr>
<th>Week</th>
<th>Lecture</th>
<th>Assignments Due</th>
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<tbody>
<tr>
<td>08/27 – 08/31</td>
<td>Fundamentals of digital logic &amp; IC design</td>
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<tr>
<td>09/03 – 09/07</td>
<td>Fundamentals of digital logic &amp; IC design</td>
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<tr>
<td>09/10 – 09/14</td>
<td>FPGA overview</td>
<td>Homework 1</td>
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<tr>
<td>09/17 – 09/21</td>
<td>Combinational logic design</td>
<td>Lab 1</td>
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<tr>
<td>09/24 – 09/28</td>
<td>Combinational logic design</td>
<td>Homework 2</td>
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<tr>
<td>10/01 – 10/05</td>
<td>Combinational logic design</td>
<td>Lab 2</td>
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<tr>
<td>10/08 – 10/12</td>
<td>Combinational logic design/Review</td>
<td>Homework 3</td>
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<tr>
<td>10/15 – 10/19</td>
<td>Sequential logic design</td>
<td>Midterm Exam</td>
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<tr>
<td>10/22 – 10/26</td>
<td>Sequential logic design</td>
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<td>10/29 – 11/02</td>
<td>Sequential logic design</td>
<td>Lab 3</td>
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<td>11/05 – 11/09</td>
<td>Sequential logic design</td>
<td>Homework 4</td>
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<td>11/12 – 11/16</td>
<td>Platform FPGA</td>
<td>Lab 4</td>
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<td>11/19 – 11/23</td>
<td>Platform FPGA</td>
<td>Homework 5</td>
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<tr>
<td>11/26 – 11/30</td>
<td>Platform FPGA</td>
<td>Lab 5</td>
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<tr>
<td>12/03 – 12/07</td>
<td>Platform FPGA/Review</td>
<td>Homework 6</td>
</tr>
<tr>
<td>12/10 – 12/14</td>
<td>No Lecture</td>
<td>Comprehensive Final Exam</td>
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