CSCE 3730 – Reconfigurable Logic

Fall 2013

Class Hours & Location: Tuesday and Thursday, 10:00am-11:20am, NTDP B192
Class Website: [http://www.cse.unt.edu/~song/csce3730/](http://www.cse.unt.edu/~song/csce3730/)

Instructor: Dr. Song Fu
Office: NTDP F250
Office Hours: Tuesday and Thursday, 4:00pm-5:00pm, or by appointment
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Teaching Assistant: Shijun Tang
TA Office: Help Lab
TA Office Hours: TBD
TA Contact: ShijunTang@my.unt.edu

Textbooks: 
FPGA-Based System Design by Wayne Wolf

The Designer's Guide to VHDL (3rd Ed.) by Peter Ashenden

Recommended Readings:

VHDL: A Starter's Guide (2nd Ed.) by Sudhakar Yalamanchili

Prerequisites: CSCE 2610: Assembly Language and Computer Organization

Course Objectives: This course is about the design of digital systems using field-programmable gate arrays (FPGAs) and hardware description languages (HDLs). We will learn the building of individual components of a computer such as ALU, register file, and RAM, and how to put them together in constructing a computer using FPGAs. Students will acquire practical working knowledge of creating digital circuits using computer-aided-design tools. The outcomes of this course are:

- Understand the concept of reconfigurable logic.
- Know how FPGA is designed.
- Have an overall view of Computer Aided Design for FPGA.
- Understand specific algorithms utilized in technology mapping, placement and routing.
- Learn how to use the VHDL hardware description language to simulate and synthesis digital circuit system.
• Be capable of using commercial CAD tools to design and simulate digital circuits.

Tentative Schedule:

Week 1     Fundamentals of integrated circuit design  
Week 2     Field-programmable gate array overview  
Week 3     FPGA logic elements, programmable interconnects  
Week 4     Implementation of combinational logic using FPGA  
Week 5     Implementation of sequential logic using FPGA  
Week 6     FPGA placement and routing algorithms  
Week 7     Midterm exam  
Week 8     Hardware description language  
Week 9,10  FPGA programming in VHDL  
Week 11    FPGA design flow in VHDL  
Week 12    FPGA behavioral design in VHDL  
Week 13,14 Finite state machine implementation in VHDL  
Week 15    FPGA-based reconfigurable systems  
Week 16    Final exam

Grading:

10% - Attendance and class participation;  
30% - Homework, lab assignments, and quizzes;  
30% - Midterm exam;  
30% - Final exam.

Every student is expected to attend all lectures, read the assigned reading before class, and participate in class discussions.

Late Policies:

Assignments are due before class on the due date. Late assignments will be penalized 10% per day, up to 3 days. No credit will be given after 3 days. Please try to finish your assignments on time.

Cooperation & Academic Honesty:

Each homework and lab assignment must be worked on individually. A submission carries with it an implicit statement that the submission is your own work. You may discuss the requirements and syntactical issues, but not solutions or designs. Violations may result in failure of the course.

Disability Policy:

The Computer Science Department and this instructor cooperate with the Office of Disability Accommodation to make reasonable accommodations for qualified students (cf. Americans with Disabilities Act and Section 504, Rehabilitation Act) with disabilities. If you have not registered with ODA, we encourage you to do so. If you have a disability for which you will require accommodation please discuss with me after class and present a written accommodation request on or before the 2nd week of class.