CSCE 3730 – Reconfigurable Logic

Fall 2010

Instructor:	Dr. Song Fu
Office:	NTRP F250
Office Hours:	Tuesday & Thursday, 10:30am – 11:30am
Email:	song.fu@unt.edu
Class Meeting Time & Location:	Tuesday & Thursday, 3:30pm-4:50pm, NTRP B158
Class Website:	http://www.cse.unt.edu/~song/csce3730/
Class Discussion Group:	csce3730fall10@googlegroups.com
Teaching Assistant:	Ademola Fawibe
TA Office Hours:	Tuesday 8:00am-10:00am and Wednesday 2:00pm-4:00pm
TA Office:	NTRP F205
Textbooks:	*FPGA-Based System Design* by Wayne Wolf Prentice Hall, 2004. ISBN: 0-13-142461-0 *The Designer's Guide to VHDL* (3rd Ed.) by Peter Ashenden Morgan Kaufmann, 2008. ISBN-13: 978-0-12-088785-9 Recommended Readings: *VHDL: A Starter's Guide* (2nd Ed.) by Sudhakar Yalamanchili Prentice Hall, 2005. ISBN-13: 978-0131457355
Prerequisites:	CSCE 2610: Assembly Language and Computer Organization
Course Objectives:	This course is about the design of digital systems using a hardware description language, VHDL. Students will be taught about the building of the individual components of a computer such as ALU, register file, and RAM, and how to put them together in constructing a computer based on FPGAs. Students will acquire practical working knowledge of creating digital circuits using computer-aided-design tools. The objectives of this course are: • Understand the concept of reconfigurable logic. • Know how FPGA is designed. • Have an overall view of Computer Aided Design for FPGA.

- Understand algorithms utilized in technology mapping, placement and routing.
- Learn how to use the VHDL hardware description language to simulate and synthesis digital circuit system.
- Be able to use CAD tools to design and simulate digital circuits.

Tentative Schedule:

Week 1 Fundamentals in Digital IC Design
Week 2 FPGA Architectures and Logic Cells
Week 3 FPGA Programming
Week 4 FPGA Implementation of Combinational Logic
Week 5 FPGA Sequential Logic Implementation
Week 6 Timing in FPGA Synchronous Cirtuits
Week 7 Midterm Exam
Week 8 Introduction to VHDL
Week 9 FPGA Design with VHDL
Week 10 FPGA Arithmetic Cirtuits
Week 11 FPGA Microprocessors
Week 12 FPGA-based System Design and Reconfiguration
Week 13 Design Examples of FPGA-based System
Week 14 Final Exam

Grading:

10% - Attendances and class participation;
30% - Written homework, lab assignments, and quizzes;
30% - Midterm exam;
30% - Final exam.

Every student is expected to attend all lectures, read the assigned reading before class, and participate in class discussions.

Late Policies:

Assignments are due before class on the due date. Late assignments will be penalized 10% per day, up to 3 days. No credit will be given after 3 days. Please try to finish your assignments on time.

Cooperation & Academic Honesty:

Each homework and lab assignment must be worked on individually. A submission carries with it an implicit statement that the submission is your own work. You may discuss the requirements and syntactical issues, but not solutions or designs. Violations may result in failure of the course.