CSCE 4610: Computer Systems Architecture

Instructor: Song Fu
My Office: F250 Discovery Park
My Phone: 940-565-2341
My Email: song.fu@unt.edu
My Web: http://www.cse.unt.edu/~song/
My Office Hours: Tuesdays 10:00-11:00am
Thursdays 10:00-11:00am

TA: Amar Maharjan
(AmarMaharjan@my.unt.edu)
TA Office Hours: Wednesdays 11:00am-12:30pm

Tentative Breakdown Of Course Grades

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Attendance and Discussion</td>
<td>5%</td>
</tr>
<tr>
<td>Homework Assignments</td>
<td>20%</td>
</tr>
<tr>
<td>2 Mid Semester Exams (No final exam)</td>
<td>50%</td>
</tr>
<tr>
<td>Term Project</td>
<td>25%</td>
</tr>
</tbody>
</table>

Prerequisites: CSCE 2610, CSCE 3612 or CSCE 3600

Primarily, you should know how a basic CPU works, assembly language programming in MIPS (or ARM) instruction, memory organization, ALU (including multiplication, division and floating point algorithms), and some understanding of compilers and runtime support, Operating system concepts like process scheduling, virtual memory, protection domains, etc.

Exams and Grading Policies: Both mid-semester exams are "open-book" format. Every exam will be graded using a "relative point" system. For each problem, the best among all the solutions presented by the students (which gets the highest grade) will be selected and all the others will be graded relative to the best solution.

ABET Course Outcomes for CSCE 4610

1. Apply metrics to evaluate performance and power requirements of modern computer systems. Represent performance using arithmetic, harmonic and geometric means.
2. Understand Amdahl’s law as applied to a single core and multicore systems.
3. Design a pipelined processor to meet design specifications.
5. Understand cache memory performance issues.
6. Understand cache memory issues in multicore systems include cache coherency management.
7. Understand hardware support for concurrency including multithreading, locks and barriers.
CSCE 4610: Computer Systems Architecture
Course Outline
Course materials are on Canvas

1. Introduction and Background  
   - What is computer architecture  
   - Instruction sets, control unit  
   - Performance evaluation  

2. Memory Systems  
   - Memory hierarchy  
   - Cache memory designs  
   - Improving cache performance  
   - Main memory and Virtual memory  
   - DRAM and SSD technologies  

3. Pipeline and out of order execution  
   - Basic design of pipelines  
   - Data and control hazards  
   - Branch prediction and dynamic scheduling  
   - Superscalar and multiple issue processors  
   - VLIW or EPIC  

4. Shared Memory Multiprocessors  
   - Mutual Exclusion and Synchronization  
   - Cache Coherency Problem and Solutions  
   - Distributed Shared Memory Systems  

5. Dataflow and multithreaded architectures  
   - Dataflow model of computation  
   - What is multithreading Scheduled Dataflow  
   - SMT and Hyper Threading  

6. Low Power Issues  


Other Useful Books: