CSCE 3730 – Reconfigurable Logic  
Fall 2011

Class Hours & Location: Monday & Wednesday, 3:30pm-4:50pm, NTDP D215
Class Website: http://www.cse.unt.edu/~song/csce3730/
Class Discussion Group: untcse3730fall11@googlegroups.com

Instructor: Dr. Song Fu
Office: NTDP F250
Office Hours: Monday & Wednesday, 1:30pm-2:30pm, or by appointment
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Teaching Assistant: Sanjay Kumar
TA Office: TBD
TA Office Hours: TBD
TA Contact: SanjayKumar@my.unt.edu

Textbooks:  
FPGA-Based System Design by Wayne Wolf  

The Designer's Guide to VHDL (3rd Ed.) by Peter Ashenden  

Recommended Readings:

VHDL: A Starter's Guide (2nd Ed.) by Sudhakar Yalamanchili  

Prerequisites: CSCE 2610: Assembly Language and Computer Organization

Course Objectives: This course is about the design of digital systems using a hardware description language, VHDL. Students will be taught about the building of the individual components of a computer such as ALU, register file, and RAM, and how to put them together in constructing a computer based on FPGAs. Students will acquire practical working knowledge of creating digital circuits using computer-aided-design tools. The outcomes of this course are:

• Understand the concept of reconfigurable logic.
• Know how FPGA is designed.
• Have an overall view of Computer Aided Design for FPGA.
• Understand specific algorithms utilized in technology mapping, placement and routing.
- Learn how to use the VHDL hardware description language to simulate and synthesize digital circuit systems.
- Be capable of using commercial CAD tools to design and simulate digital circuits.

Tentative Schedule:

Week 1     Fundamentals in Digital IC Design
Week 2     FPGA Architectures and Logic Cells
Week 3     FPGA Programmable Interconnect
Week 4     FPGA Implementation of Combinational Logic
Week 5,6   FPGA Sequential Logic Implementation
Week 7     Timing in FPGA Synchronous Circuits
Week 8     Midterm Exam
Week 9     Introduction to VHDL
Week 10    Xilinx Spartan FPGA & ISE
Week 11    FPGA Design with VHDL
Week 12    FPGA Arithmetic Circuits
Week 13    Finite State Machines
Week 14    FPGA-based System Design and Reconfiguration
Week 15    Design Examples of FPGA-based System
Week 16    Final Exam

Grading:

10% - Attendances and class participation;
30% - Written homework, lab assignments, and quizzes;
30% - Midterm exam;
30% - Final exam.

Every student is expected to attend all lectures, read the assigned reading before class, and participate in class discussions.

Late Policies:

Assignments are due before class on the due date. Late assignments will be penalized 10% per day, up to 3 days. No credit will be given after 3 days. Please try to finish your assignments on time.

Cooperation & Academic Honesty:

Each homework and lab assignment must be worked on individually. A submission carries with it an implicit statement that the submission is your own work. You may discuss the requirements and syntactical issues, but not solutions or designs. Violations may result in failure of the course.