CSCE 4730: VLSI Design
(and CSCE 5730: Digital CMOS VLSI Design)

Instructor: Saraju Mohanty
Office: NTDP F247
Office Hours: MW 3:00--4:00pm
Phone: 940-565-3276

Semester: Fall 2011
Time: MW 5:00--6:20pm
Place: NTDP B192
E-mail: saraju.mohanty@unt.edu

Course Description:
Introduction to VLSI design using CAD tools, CMOS logic, switch level modeling, circuit characterization, logic design in CMOS, systems design methods, test subsystem design, design examples, student design project.

Textbook:
Digital Integrated Circuits by Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, Prentice Hall, ISBN: 0130909963.

References:
Principles of CMOS VLSI Design: A Systems Perspective by Neil Weste and David Harris, Addison Wesley.

Learning Outcomes:
By the end of this course a students will:

1. Understand the concept of MOS transistor.
2. Understand the operational characteristics of MOS transistor.
3. Understand the Power dissipation mechanisms in MOS transistor.
4. Understand the CMOS Process and Technology.
5. Able to use commercial CAD tools to design and simulate digital circuits.

Course Requirements:
Attendance: Mandatory
Exams: 3 equal weightage tests; one at the end of each month.
Assignments: There will be 4 to 6 required assignments.

For More Information:
Website: https://ecampus.unt.edu

Disability Accommodation:
The University of North Texas complies with Section 504 of the 1973 Rehabilitation Act and with the Americans with Disabilities Act of 1990. The University of North Texas provides academic adjustments and auxiliary aids to individuals with disabilities, as defined under the law. Among other things, this legislation requires that all students with disabilities be guaranteed a learning environment that provides for reasonable accommodation of their disabilities. If you believe you have a disability requiring accommodation, please see the instructor and/or contact the Office of Disability Accommodation at 940-565-4323 during the first week of class.

A Tentative Calendar and Topics:

Week	Topic
1	MOS transistor theory
2	MOS transistor theory
3	CMOS processing technology
4	Test 1
5	Circuit Characterization
6	Circuit Characterization
7	Power Dissipation
8	Power Dissipation
9	Test 2
10	Clocking Strategies
11	Design methods and tools
12	Design methods and tools
13	CMOS testing
14	Test 3
15	System Design Examples, Presentation and Demo
16	System Design Examples, Presentation and Demo

Teaching Assistant:

TBA

Course policy:

- **Attendance for this course is mandatory**. In the case of absence due to unavoidable reasons, substantial documented evidence must be provided.
- Several **assignments** including exercise problems and design works will be given. The written or typed solutions for exercise problems and reports for design works must be submitted in the class **at the beginning of lecture** of announced deadline, else **there will be late penalty of 20%.** Under no circumstances late assignment will be accepted three days after deadline and score for such assignment will be zero.
- **There will be three tests of equal weightage.** There will be no final test. The tests will be approximately evenly spaced throughout the semester. The tests will be conducted in the same lecture room. The dates of the tests will be announced right on the 1st lecture, and the test dates will not be changed under any circumstances.
- Any makeup test will not be given unless substantial documented evidence is provided for a reasonable excuse of absence. In the absence of the documented evidence the score for the test will be zero.
- Any questions regarding the test grades should be clarified **a week of returning the test**. If no complaint is formulated within one week after the grades are posted on the course web page, **it will be considered that the student accepted the grade and the corresponding grades are considered definite**.
- No student shall be compelled to attend class or sit for a test on a day or time prohibited by his or her religious belief.

- Dishonesty in this class will be handled as per the University of North Texas policy (http://www.unt.edu/csrr).
- If a student needs any special accommodations according to the American Disability Act, he or she should let the instructor know.
- **Student Evaluation of Teaching Effectiveness (SETE) Completion:** The students should complete the SETE, which is a short survey. The SETE is a requirement for all organized classes at the UNT. SETE will be made available for the students at the end of the semester to provide them a chance to comment on how this class is taught. The instructor is very much interested in the constructive feedbacks from the students to continually improve his teaching of this course.

Tests Dates:

Test No.	Date	% of Final Grade (for CSCE 5730)	% of Final Grade (for CSCE 4730)
Test 1	28th September 2011 (Wed)	25	30
Test 2	26th October 2011 (Wed)	25	30
Test 3	28th November 2011 (Mon)	25	30

Grade Distribution:

Items	% of Final Grade (for CSCE 5730)	% of Final Grade (for CSCE 4730)
Tests	75	90
Assignments	10	10
Project/Survey	15 (abstract + report + presentation - 3+8+4) **Deadlines**: Abstract: 31st Oct 2011 (Mon) Report: 23rd Nov 2011 (Wed) Presentation: 30th Nov 2011 (Wed), 5th Dec 2011 (Mon), and 7th Dec 2011 (Wed)	NA

Grading Policy:

A >= 90; 90 > B >= 80; 80 > C >= 70; 70 > D >= 60; F < 60

Notice: (1) Grading method may be changed if the CSE Department so decides. (2) NO border grade concession.