Instructor: Colleen Bailey PhD, NTDP B252, Colleen.Bailey@unt.edu

Office Hours: R TBD or by appointment

Lab: R 5:30 PM to 8:20 PM; NTDP B207

TA: Veena Chidurala, NTDP B251, veenachidurala@my.unt.edu, R 4:00 PM to 5:00 PM

Co-requisite: EENG 2710 Digital Logic Design

Course Description: Provides the students an opportunity to design and debug digital circuits using logic gates and flip-flops, SSI, MSI integrated circuits and PLAs. The course also reinforces the concepts they learn in combinational and sequential logic and enhances report writing skills of the students.

Course Outline:

Session 1 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . Number System Recitation
Session 2 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . Introduction to Logic Simulators
Session 3 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . TBD
Session 5 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . TBD
Session 4 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . TBD
Session 6 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . TBD
Session 7 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . TBD
Session 8 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . TBD
Session 9 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . TBD
Session 10 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . TBD

Grading:
Attendance REQUIRED TO PASS
Lab Reports 100%

Course Policies:

- Lab Reports are due at the beginning of class. Reports turned in after class will be penalized 50%. No reports will be accepted after 24 hours.
- You have one week to contest any grade once the report is returned.

Canvas: Course material and grades will be maintained on the course Canvas site. You should check this page often to keep current on important information. https://unt.instructure.com

Lab Components: Each student is provided with one set of components for the semester. You are responsible for bringing them to lab each week. Any lost or broken components will need to be replaced by the student. The provided breadboard, wires, and box will be used throughout your time in the UNT EE program.
Rights and Responsibilities:

- Students are expected to communicate to the instructor any issue regarding their performance in class ahead of time.

- Attendance is required and will be recorded each class. Students aware of an authorized absence (religious observance, military service, official university function, etc.) should notify the instructor as soon as possible according to UNT Policy 15.2.5.

- Students with disabilities should inform the instructor of their needs at the beginning of the semester according to UNT Policy 18.1.14 in order to receive proper attention and accommodations.

- Cheating and academic dishonesty will not be tolerated. Any student found to have participated in academic dishonesty will receive an F in the class, and may be subject to further disciplinary action. Acts of academic dishonesty include: academic fraud (e.g. changing solutions to appeal a grade), copying or allowing one’s work to be copied, fabrication/falsification, plagiarism, sabotage of others’ work, substitution (e.g. taking an exam for someone else). For more details, see UNT Policy 18.1.16.

- Letter grades will not be assigned until the end of the term, after the final exam has been graded. Any letter grade assignment posted before the end of the class should be regarded as tentative and subject to change.