University of North Texas
Department of Electrical Engineering
EENG 2910 – Digital System Design
Fall 2017

Instructor: Dr. Shengli Fu, Nicholas Tompkins
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Class Hours: Wednesdays 2:30PM - 5:20PM
Classroom: NTDP B288
Office: NTDP B238
Office Hours: Tuesdays 9:30AM – 10:30AM & Thursdays 9:30AM – 11:30AM or by appointment

Course Description:
Digital system design projects provide students substantial experience in logic analysis, design, logic synthesis in VHDL, and testing. Project documentation including all the phases of project cycle from requirement analysis to testing as well as a project presentation providing the students an opportunity to enhance their communication and presentation skills are essential components of this course.

Prerequisite: Digital Logic Design (EENG 2710)

Reference Textbooks:

Learning Outcomes:
Student will:
1. Demonstrate an understanding of project life-cycle through semester-long hands-on projects.
2. Design complex digital systems consisting of combinational and sequential circuits starting from a word description that performs a set of specified tasks and functions.
3. Demonstrate project planning and scheduling skills.
4. Develop skills, techniques and learn state-of-the-art engineering tools (such as Xilinx tools, VHDL) to design, implement and test modern-day digital systems on FPGAs.
5. Design control units as a state machine for complex systems.
6. Analyze the results of logic and timing simulations and to use these simulation results to debug digital systems.
8. Research design ideas and collect reference material that relates to their projects.
9. Defend their projects orally with good presentation skills.
10. Thoroughly document all phases of their project.
11. Understand engineering design, the steps involved, and carry out engineering design principles in the design of a simple processor.
12. Demonstrate an understanding of ethical and professional issues as related to their projects.

General Policy:

- A perfect attendance is recommended for those aspiring to get good grades because there will be constant evaluation of skills.
- Announcements about the course will be posted on BlackBoard. It is therefore your responsibility to always check your BlackBoard.
- Small project reports are due at the beginning of class on the due date.
- All reports must be typed – no hand-written reports will be accepted for grading.
- All small projects are individual work unless otherwise stated. Simply copying others’ work will be treated as a violation of academic honesty.
- Tardiness: If you arrive late, please enter quietly and sit down.
- Cell Phones: Please remember to turn off phones prior to class or put them in silent mode – (for emergency purpose only).
- Students are strongly encouraged to get to know each other.
- It is the responsibility of the students with certified disabilities to provide the instructor with appropriate documentation from the Dean of Students Office (see http://www.unt.edu/oda).
- Please visit http://www.unt.edu/csrr/ for your rights and responsibilities.
- Important dates and deadlines are available at http://registrar.unt.edu/registration/fall-registration-guide

Grading Policy:

- Exam and/or Quizzes: 10%
- Small Projects: 60%
- Final Project: 30%
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<th>Week</th>
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<th>Topic</th>
<th>Assignment</th>
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<td>Introduction to Digital System Design, VHDL, and Basys2 Board</td>
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<td>2</td>
<td>XXX</td>
<td>Combinational Logic Design (Discuss Report Writing)</td>
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<td>Introduction to Course Project (Select Project Teams)</td>
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<td>State Machine and Sequential Logic Design</td>
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